IN THE SPECIFICATION

Please amend the indicated paragraph as follows:

[0062] In one embodiment, the second metal layer 508 is etched in the chamber 300 by providing 0-5000 sccm of BCl_3 and 50-500 sccm of chlorine comprising gas, such as Cl_2/HCl. Optionally, O_2 and/or He may also be provided to the processing chamber 300 at flow rates between 50-500 sccm. The BCl_3 is first ~~exited~~excited in the remote plasma source 384 by coupling about 1-30 kWatts of power thereto. A plasma is formed from the gas mixture within the chamber 300 by applying about 5-30 kWatts of RF power to the gas distribution plate assembly 318. The bias power additionally provides activation energy to etch the second metal layer 508. The metal etch step 412 is generally selective to the N+/α-silicon layer 506, which may be used as an etch stop. In one embodiment, step 412 includes delivering about 1000 sccm of BCl_3 to the remote plasma source 384, energizing the BCl_3 with about 5 kWatts of power, delivering about 2000 sccm of Cl_2/HCl to the processing chamber 300, and biasing the gas distribution plate assembly with about 10 kWatts of RF power. Step 412 is generally performed at a pressure between about 10-500 mTorr and at a substrate temperature of about 100 ± 60 degrees Celsius. The metal etch step 412 produces a film stack 500B that is depicted in Figure 6. The use of the ~~remove~~remote plasma source 384 to active, excite and/or dissociate at least portion of the process gases allows for higher processing temperatures, which, in concert with the capacitive power applied between the gas distribution plate assembly and substrate support, thereby allow the film stack to be efficiently etched with reduced temperature excursion due to plasma heating.

[0066] Following the silicon etching step 414, a partial ashing step 416 is performed in the chamber 300 on the film stack 500C. The partial ashing step 416 removes the thinner section 512 of the photoresist layer 510 to expose a portion 530 of the second metal layer 508 between the thicker sections 514 of the photoresist. In one embodiment, the thinner section 512 of the photoresist is

removed by ashing to expose a portion ~~532~~530 of the underlying second metal layer 508.

[0067] One example of a suitable ashing process comprises providing between about 500-10,000 sccm of O_2 to the processing chamber 300 from the gas source 386. N_2 may additionally be provided to the processing chamber. A plasma from the O_2 within the chamber 300 by applying about 5-30 kWatts of RF power to the gas distribution plate assembly 318. The ashing step 416 is stopped when the underlying second metal layer portion ~~532~~530 is exposed. In one embodiment, step 416 includes delivering about 4000 sccm of O_2 to the processing chamber 300, and biasing the gas distribution plate assembly with about 10 kWatts of RF power. Step 414 is generally performed at a pressure between about 10-1,000 mTorr and a substrate temperature of about 100 ± 60 degrees Celsius. The partial ashing step 416 produces a film stack 500D that is depicted in Figure 8.

[0068] The exposed second metal layer portion ~~523~~530 of the film stack 500D is etched at step 418 in the chamber 300. The metal etching step 418 exposes a portion 534 of the underlying a-silicon layer 504. In one embodiment, the metal etch step 418 is substantially identical to the process parameters of step 412. The metal etching step 418 produces a film stack 500E that is depicted in Figure 9.

[0069] At step 420, the a-silicon layer 504 and the N+/a-silicon layer 506 of the film stack 500E are etched in the chamber 300. The silicon etch step 420 breaks completely through the N+/a-silicon layer ~~504~~506 and partially through the ~~N+/~~a-silicon layer ~~506~~504, thus forming a channel 524 in the ~~N+/~~a-silicon layer ~~506~~504. The channel 524 includes a thin strip 526 of ~~N+/~~a-silicon material covering the gate insulator layer 520 above the gate metal layer 502. The silicon etching step 420 produces a film stack 500F that is depicted in Figure 10. In one

embodiment, the silicon etching step 420 is substantially identical to the process parameters of step 414.